ABSTRACT

A system and method to establish the lock point of a digital synchronous circuit (e.g., a DLL) at the center of or close to the center of its delay line to provide for extra tuning range in the event of voltage, temperature and frequency changes after the initial lock is established. The delay line receives a clock signal as its input and imparts a given delay to the clock signal to generate a feedback clock that is synchronized or "locked" with the clock signal. The synchronous circuit is configured to selectively use either a reference clock or its inverted version (an inverted reference clock) as the clock signal input to the delay line based on a relationship among the phases of the reference clock, the inverted reference clock, and the feedback clock. A delayed version of the feedback clock may be used during determination of the phase relationship. The selective use of the opposite phase of the reference clock for the input of the delay line results in centralization of the lock point for most cases as well as improvement in the tuning range and the time to establish the initial lock, without requiring an additional delay line or without increasing the size or changing the configuration of the existing delay line.